A Digital Power Amplifier for 1.5 T

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Audience: Those interested in RF technology and parallel transmission.

Purpose: Parallel transmission (PTx) is an ongoing research in magnetic resonance imaging (MRI). In order to implement PTx in MR scanners multiple high power linear amplifiers are needed. In order to reduce the cost of the design, recently, using on coil switched mode power amplifiers are proposed [1]. In this work, we design a 64 MHz Class-E power amplifier for on coil excitation purpose. The amplifier embodies also the transmit coil as the load network of the structure. This simplifies the circuit further and enables implementation of the design in commercial scanners.

Methods: The amplifier structure is given in Figure 1. The structure consists of field programmable gate array (FPGA), gate driver, power transistor, RF choke inductor and load network. The amplifier is controlled by the signals from an FPGA (ML509EVB), which are fed to the gate driver in low voltage differential signaling (LVDS) form. The gate driver has two functions: First to convert the LVDS signals to square pulses of 0-6Volts to create gate voltage; second to provide charge/discharge current to the input capacitance of the power transistor in order to switch it on and off at the operating frequency. Two different drivers are designed: One of the drives was implemented using parallel the current feedback operational amplifiers (THS3202) and the other is driving two 1W NMOS (RFM01U7P) transistors differentially in cascode configuration. The power transistor is the BLF871 from NXP which is a 100W laterally diffused metal oxide semiconductor field effect transistor (LDMOSFET). The RF choke inductor is a quarter wavelength coaxial cable terminated with bypass capacitors at supply side and creates high impedance at the drain port of the power transistor. It causes the supply deliver constant DC current to the load network and isolates the supply from the radio frequency (RF). The load network consists of a shunt capacitor and a series RLC resonant circuit at the drain port. The shunt capacitor is adjusted such that at time the power transistor switches on, both voltage and current of the shunt capacitor are zero. This ensures maximum efficiency. The RLC circuit adjusts the output waveform of the amplifier. The transmit coil (6cm diameter) and its tuning capacitors forms the load network. The load resistance is the equivalent resistance of the coil representing losses in the system. The transmit coil is designed such that the body loss is the dominant factor in this equivalent resistance. Note that a separate load resistance was not used. The amplifiers circuits are shown in Figure 2.

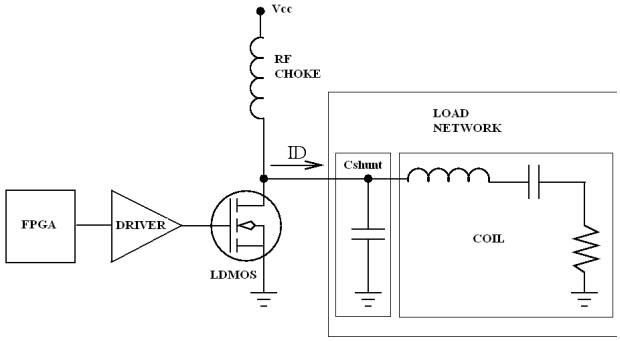

Figure 1: Amplifier circuit diagram

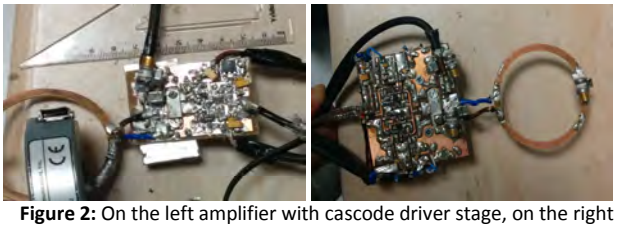

Figure 2: On the left amplifier with cascode driver stage, on the right amplifier with parallel op-amps.

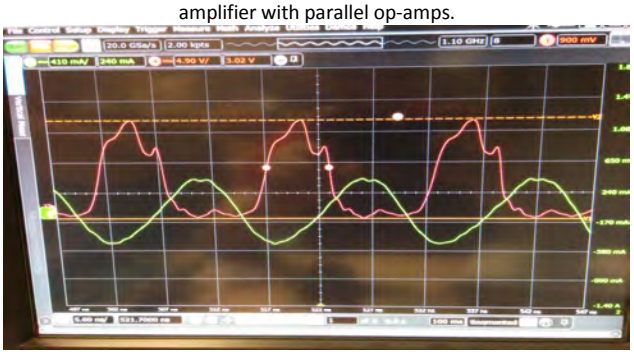

Figure 3: Red line is the drain voltage and green line is the load current

V_{supply}	I_{supply} (A)	I_{coil} (p-p A)	P_{in}	P_{out} (calc.)	Efficiency
5	0.54	0.884	2.7	1.85	68
10	1.02	1.772	10.2	7.42	72.7
15	1.47	2.610	22.05	16.09	72.97
20	1.87	3.291	37.4	25.58	68.4
25	2.26	3.963	56.5	37.1	65.7

Table 1: Measured input power and calculated output power and the drain efficiency for different bias conditions

Results: A FCC F-61 current probe is placed on the transmit coil to measure the output power of the amplifier. The coil and the probe combination creates an 18.9Ω resistive loading which resembles the loading effect of a 18.9 ohm matched coil. The Class-E behavior of the amplifier is tested in burst mode operation in order not to damage transistor and the chip resistors. The power from the supply is measured for a short duration (<1s) of time when driving the amplifier with square wave. The drain voltage and the load current for 5V supply voltage are shown in Figure 3. The reason for low biasing is the limitation of active oscilloscope probe. Finally, an output power of 56.5W gathered with a drain efficiency of %65.7 which is shown in Table-1.

Discussion and Conclusion: We have shown that the Class-E type amplifier has the potential for MRI application as a **digital power amplifier**. The **digital control, higher efficiency and integration with the transmit coil** appear as the strength of the Class-E amplifier. LDMOSFETs are vastly available on the market with reasonable prices. The driver circuit design is very critical in order to have appropriate rise/fall times of the square pulses at the operating frequency. The driver circuits built in this work can easily be adapted to higher frequencies. A feedback loop with sniffer coil is needed for measuring the amplifier parameters. The dependency of the output capacitance of the transistor on the bias affects the efficiency of the amplifier. Moreover, shielding of the amplifier is required in order to decouple the amplifier from the radiation from the transmit coil. Due to the calibration difficulties at low load impedance (≤4Ω), measurements are done using 18.9Ω load resistance which can be high for the driven coil but is possible coil resistance for a bigger loop. As a future work, measurement setup will be adapted to low impedance measurements.

In this work, we have designed a single amplifier as a feasibility study. In the future work, we plan to build a 36-channel transmit array of Class-E amplifiers which are controlled totally using a digital hardware.

References: [1] Gudino N, et al. Proc. ISMRM 2014 (Abstract 545)

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