Design of multi-channel switching system for matrix coils

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Introduction: Matrix coils were recently developed for shimming and imaging¹⁻³. In those approaches each coil element was driven by a separate amplifier. The number of amplifiers therefore was necessary equal to the number of coil elements. A dynamically controlled adaptive shimming method has been introduced recently ⁴. In this method the current path is altered by metal-oxide-semiconductor field-effect transistors (MOSFETs) and a high number of coil elements are controlled by one single amplifier. Here we present a hardware design of multi-channel switches for a dedicated matrix gradient coil. The switching system is used to control the combination of the matrix coil elements. The configuration of the matrix coil is constant for a given gradient pulse and can be changed between the pulses. This way many coil elements can be driven by a single amplifier and the total number of gradient amplifiers required to drive a matrix gradient system can be reduced.

Method: Fig. 1 shows the block diagram of multi-channel switching system. The system consists of a controller and a number of analog switches. The controller contains a microcontroller (XC886CM, Infineon) and a Complex Programmable Logic Device (CPLD, XC9572XL, Xilinx). The analog switches are designed to be placed in the immediate vicinity of the matrix coil elements inside the magnet bore. To keep connections short, the CPLD is also located inside the magnet. The presented design can reach a total of 64 channels and is only limited by the quantity of user IO pins of chosen CPLD. Coil setting for the individual channel combination is sent via a serial interface from a PC to

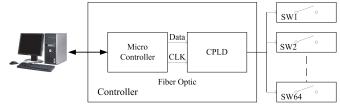


Fig. 1 Block diagram of multi-channel switching system

the microcontroller ahead of the experiment. The microcontroller loads these parameters onto the CPLD via serial interface. After download, the CPLD immediately applies the code settings to the individual analog switches. The serial communication interface between microcontroller and CPLD only consists of data and clock line. An optical fiber cable is used for connection to avoid noise interference. To minimize the induced radio frequency noise during the MR signal acquisition period, the clock is activated only at the communication period.

Fig. 2 presents the schematic of one analog switch. Each switch contains two MOSFETs (IXFK360N15T2, IXYS), a high-side MOSFET driver (IRS21850S, International Rectifier), a timer and a current source. The maximum working voltage of MOSFET is 150V and the maximum working current is 160A. The bootstrap circuit is used to drive the MOSFETs. The timer circuit in combination with the current source (5; current source instead of the 100k/1W resistor) charges the bootstrap capacitor periodically and generates the power supply for the floating driver output circuit. To work under the condition of the low output voltage of gradient amplifier, a negative voltage referenced current source is used.

Results & Discussion: The system was tested experimentally with a dual channel concept design inside a 3T MR system. The photo of system is presented in Fig. 3. The maximum current for testing was limited by the available power source to 35A. The realized setup for switching high currents switched correctly following the coil setting code. A maximum current of 100A will be tested, when the appropriate gradient amplifier capable to adapt to different load condition becomes available. Due to its modular design, the number of channels can be customized in future

systems by choosing the appropriate number of analog switches. With few modifications the analog switch can also be used for low voltage gradient amplifiers with two different power supplies or as an overcurrent protection circuit.

References: 1. Juchem C, et al., Proc.ISMRM19 (2011), 97; 2. Juchem C, et al., Proc.ISMRM19 (2011), 716; 3. Jia F, et al., Proc. ISMRM21 (2013), 0666; 4. Harris C, et al., Proc. ISMRM21 (2013), 0011; 5. International Rectifier. Application note, AN-978.

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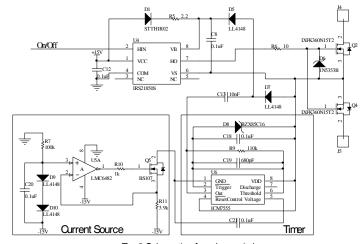


Fig. 2 Schematic of analog switch



Fig. 3 Photo of conceptual design of switching system