On the Optimum Source Impedance for MRI Phased Array Coils

Paul Joseph Cassidy[1]
[1]School of Engineering, Griffith University, Gold Coast, QLD, Australia

Introduction

Typically phased array coil elements are impedance matched to a source impedance of 50 Ω using a lumped-element quarter wave transformer circuit comprising of a matching capacitor C_m and matching inductor L_m. Each element is subsequently mismatched to the low input impedance of a preamplifier, typically < 5 Ω, for preamplifier decoupling (1). The choice of 50 Ω source impedance seems to be governed by optimisation of the preamplifier noise figure, preamplifier gain and the availability of 50 Ω RF components and measurement equipment. Recent advances in CMOS low noise amplifiers suggest that lower noise figures can be obtained at source impedances greater than 50 Ω (2). The aim of the present work is to explore the issue of source impedance for optimum phased array performance based on preamplifier decoupling, preamplifier noise figure and preamplifier gain.

Analysis

Impedance Matching & Preamplifier Blocking Impedance: A phased array coil element may be represented by the equivalent circuit shown in **Fig. 1**, where R_p is the input impedance of the preamplifier (Ω), R_s is the source impedance of the RF system (Ω) and ω is the Larmor frequency (rad/s). The match inductance L_m (H), match capacitance C_m (F) and preamplifier blocking impedance Z_{block} (Ω) can be calculated using Eqs.[1-3] (1).

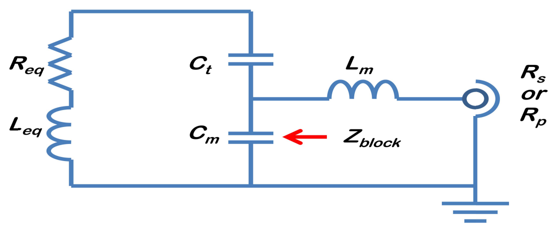

Figure 1. Circuit model of a phased array coil element.

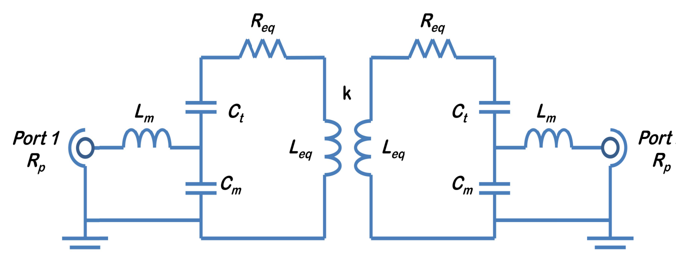

Figure 2. Circuit model of a pair of coupled phased array coils.

Preamplifier Decoupling: A pair of coupled identical phased array coils may be represented by their equivalent circuit models shown in **Fig. 2**, where k is the coupling coefficient. The degree of decoupling can be determined by Eq.[4] (3,4).

Preamplifier Noise Figure & Gain:

The minimum noise factor for a CMOS common-source low noise amplifier (LNA) is given by Eq.[5]. Q_{opt} is given by Eq.[6], where ω_0 is the operating frequency, ω_T is the unity current gain (cut-off) frequency, c = j0.395 is the gate and drain noise current correlation coefficient, $\alpha = g_m/g_{do}$, g_m is the device transconductance, g_{do} is the zero-bias drain conductance and γ and δ are coefficients of channel and gate induced noise respectively (2.5). Q is also given by Eq.[7], where C_{gs} is the gate-source capacitance and R_s is the source impedance (5). The effective transconductance of the common-source LNA under perfect matching conditions is given by Eq.[8] (5).

$$L_m = \frac{\sqrt{R_s R_{eq}}}{\omega} \quad \textbf{[Eq.1]} \qquad C_m = \frac{1}{\omega\sqrt{R_s R_{eq}}} \quad \textbf{[Eq.2]} \qquad Z_{block} = Q^2 R_p = \frac{\omega^2 L_m{}^2}{R_p} = \frac{1}{\omega^2 C_m{}^2 R_p} = \frac{R_s R_{eq}}{R_p} \quad \textbf{[Eq.3]} \qquad S_{21} = 20\log_{10}\left[\frac{2\omega k L_{eq}}{R_{eq} + Z_{block}}\right] \quad \textbf{[Eq.4]}$$

$$F_{\min} = 1 + \frac{\gamma}{\alpha}\left(\frac{\omega_0}{\omega_T}\right)\frac{2\delta\alpha^2}{5\gamma}Q_{opt} \quad \textbf{[Eq.5]} \qquad Q_{opt} = \sqrt{1 + 2|c|\sqrt{\frac{5\alpha}{\delta\alpha^2} + \frac{5\alpha}{\delta\alpha^2}}} \quad \textbf{[Eq.6]} \qquad Q = \frac{1}{\omega_0 C_{gs} R_s} \quad \textbf{[Eq.7]} \qquad G_{m,eff} = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right) \quad \textbf{[Eq.8]}$$

Discussion

Preamplifier blocking impedance and hence preamplifier decoupling improve with increasing R_s as shown by Eqs.[3,4]. For CMOS LNA's Eqs.[5-7] demonstrate that the minimum noise factor F_{min} improves with increasing R_s. However, the price paid for achieving a minimum noise factor by increasing R_s is a reduction in the effective transconductance and hence gain of the preamplifier, as described by Eq.[8]. This may appear at first inspection to be a high price to pay, but adequate gain can be achieved by cascading gain stages, and it is well known that the noise factor of the first gain stage dominates the overall noise factor of a cascaded amplifier (6). Clearly experimental validation is required to support the case for moving to a higher source impedance, but it is hoped that the arguments presented here will lead researchers to explore the optimum source impedance and semiconductor technology for MRI phased array LNA's. Finally, the authors note that the noise factor improvements afforded by increasing source impedance for CMOS LNA's may also be afforded by GaAs FET LNA's as suggested in Fig. 1a of ref (7).

References

1. Roemer et al. The NMR phased array. MRM 16,192-225 (1990)
2. Belostotski & Haslett. On selection of optimum signal source impedance for inductively degenerated CMOS LNAS. IEEE CCECE/CCGEL, 584-589 (2006)
3. Choma & Chen. Feedback Networks Theory and Circuit Applications. World Scientific. p242 (2007)
4. Boctor. Electric Circuit Analysis. Prentice-Hall Intl. Inc. p.710 (1987)
5. Allstot et al. Recent advances and design trends in CMOS RF IC's. Intl. J. High Speed Electronics and Systems. 15(2):123-174 (2005)
6. Friss. Noise figures of radio receivers. Proc. IRE 32 419-422 (1944)
7. Beck. Noise parameter extraction in the design of low noise amplifiers (LNA) for MRI. Proc. ISMRM 16, 1111 (2008)