Lots of Loops: Constructing a Highly Parallel Brain Array Coil

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Introduction: Parallel detection of the MRI signal with multiple receive-only surface coils has proven valuable for increasing image sensitivity and acquisition speed and has driven the design of MR receive arrays with an increasing number of elements [1-4]. The high degree of parallelism requires systemized design, construction and testing in order to implement the large number of tuned receive circuits with minimal mutual interaction and has altered the workflow of receive coil construction. The main aim of this educational e-poster is to inform MRI researchers about the basic procedures for phased-array construction and describe an optimized protocol for constructing, tuning and decoupling a highly parallel array coil. We demonstrate the protocol with on-bench video presentations of the construction of a 32-channel brain array.

Material and Methods: The multimedia presentation follows the steps of array coil construction. We show tips, tricks and pitfalls during the construction process, starting with how to design a coil former and ending with test imaging. Our example array coil is a 32ch pediatric brain array with a deep posterior segment (28ch, loop dia:~7cm), ►Fig.1, and a separate "frontal paddle" over the forehead (4ch). The helmet shape was taken by dilating the 95% contour of averaged MR volume images to accommodate 3mm foam padding and was realized using an ABS 3D printer. The layout of the wire (16awg) circular coil elements consisted of a hexagonal and pentagonal tiling pattern [4]. Each loop incorporates two capacitors, with a conventional matching with the coax cable across one capacitor. An active detuning circuit was formed across the match capacitor using a variable inductor (Coil Craft, Cary, IL, USA) and a PIN diode (MA4P4002B-402, Lowell, MA, USA) (►Fig.2). We pre-adjusted the traps using a sniffer probe (►Fig.2) under *S*11 measure when the PIN diode was forwarded biased.

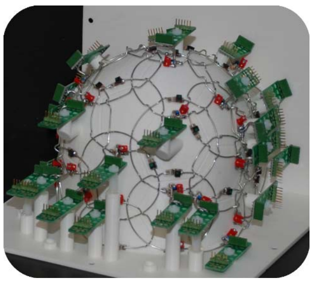
Fig.1: Populated Coil Helmet.

The coil was tuned using a double probe (*S*21 measure). The loops were matched to the load impedance designed to minimize the noise figure of the preamplifiers. After tuning we fine-adjust the active-detuning trap using the double probe (►Fig.3, red trace=tuned, blue trace=detuned). Neighboring coils are critically overlapped to reduce mutual coupling (controlled via *S*21 measure directly plugged into the preamp socket of an adjacent coil pair, ►Fig.4). The input impedance of the preamplifiers was transformed by the 4.2cm coax to provide a low impedance across the PIN diode and thus a high impedance in the loop (preamp decoupling). This was controlled via a double probe *S*21 measure (►Fig.5, blue trace).

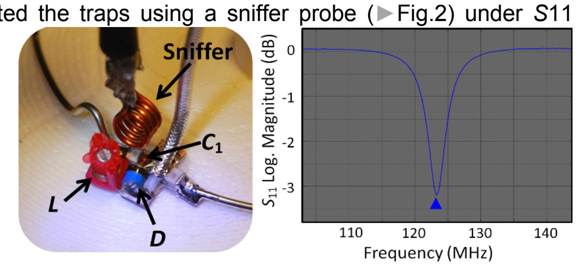

Fig.2: Active detuing pre-adjustment via sniffer probe.

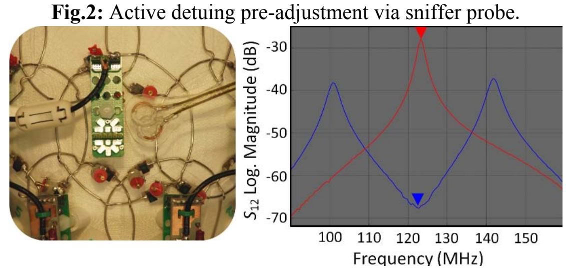

Fig.3: Tuning(red) and active detuning (blue) via double probe.

Results: The ratio of Q_U/Q_L of a loop (surrounded by six non-resonant neighbors) was 231 / 44 = 5.25. Thus, the noise is dominated by the sample for the constructed coil. Coupling between nearest neighbor elements ranged from 15dB to 21dB with an average of 17dB. This could be improved with an additional reduction of 21dB via preamp decoupling. Furthermore, active PIN diode decoupling between tuned and detuned states resulted in 46dB isolation.

Discussion: The video presentation provides a step-by-step visualization of the array construction method with the measurement results (network analyzer traces) and commentary about each step. The example array coil is an array of overlapped loops, with decoupling minimized by critical overlap, but the workflow applies to other forms of decoupling such as shared impedances. The design considerations of the layout of the elements and the size adjustments needed to meet the desired number of channels. It can be done digitally using a CAD program, as in our case, or by cutting the hexagons and pentagons from paper or cardboard and physically laying them out on the coil former [4].

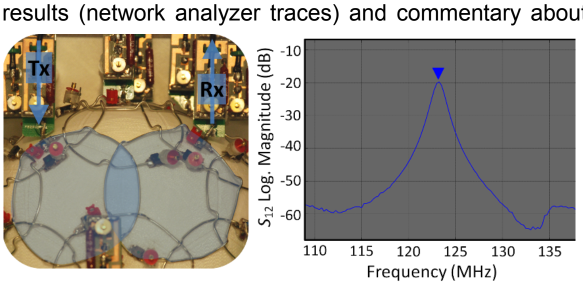

Fig.4: Geomertical decoupling measurement with cable direct plugged into preamp socket. The overlapped area was optimized under S21 measure for each adjacent pair.

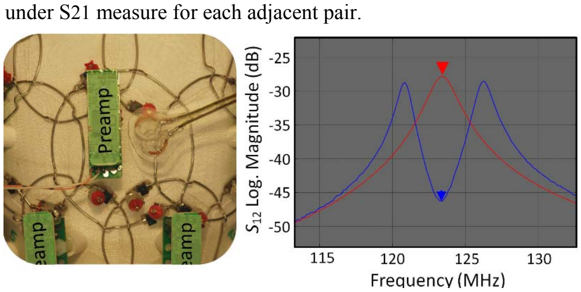

Fig.5: Preamp decoupling (blue) and tuned element without preamp presence (red) using the double probe in S21 measure.

We used wire loop elements to populate the array providing overall spatially sparser conductors, so that eddy currents and copper loading can be significant reduced compared to a circuit board conductors [3,5].

Optimization of the preamplifier decoupling is a critical step in constructing highly parallel arrays. The preamplifier/coil circuit is designed so that the preamplifier performs a high-impedance voltage measurement across the loop. The output circuitry (match + coax + preamplifier) forms a series high impedance in the tuned loop reducing current flow and thus reducing inductive coupling with other loop elements. We implement this by using the LC circuit of the active detuning trap, where the impedance of the preamplifier was transformed to a short across the diode of the detuning LC circuit, resulting in a high serial impedance in the coil loop. This is an elegant confluence of two functionalities into one circuit.

References: [1] Schmitt M *et al*.; MRM (2008) 59:6,1431-9. [2] Hardy CJ *et al*.; JMRI (2008) 28:1,1219-25. [3] Wiggins GC *et al*.; MRM (2009) 116:7,1332-5. [4] Wiggins GC *et al*.; MRM (2006) 56:1,216-23. [5] Kumar A *et al*. MRM (2009) 61:5,1201-9. [6] Roemer PB *et al*. MRM (1990), 16:2,192-225.