Digitally Controlled µ-Chip Capacitor Array for an Implantable Multiple Frequency Coil

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Introduction: Nuclear magnetic resonance (NMR) imaging and spectroscopy are capable of the non-invasive monitoring of implanted bio-artificial tissue constructs. The most direct and sensitive method that is currently used to isolate the NMR signal of the tissue construct is to implant an NMR receiver coil around the construct and remotely monitor the NMR signal response of important metabolite nuclei (1,2,3). This method is only effective at providing high signal sensitivity at a single NMR frequency thereby limiting the measurements of the metabolic signature of the tissue-construct to that of a single nucleus. Current techniques for acquiring NMR measurements of multiple nuclei suffer a significant reduction in signal sensitivity at some of the nuclei to allow optimum measurement at a single frequency.

We propose a fabricated, integrated chip design based on CMOS technology that will be used as a digitally controlled capacitor array coupled with a 20 nH NMR coil and used as a highly sensitive, multiple-frequency, wirelessly controlled implantable coil. This capacitor array chip will replace the fixed ceramic chip capacitors that are currently implemented within existing single resonant frequency NMR coils. As shown Fig. 1a, this capacitor array is part of a microchip (µ-chip) that consists of the digitally controlled capacitor (D-cap) array, a clock and data recovery circuit, a microcontroller (µ-C) with memory bank and a battery management system (BMS) to enable long term monitoring of bio-artificial tissue constructs. The NMR coil is connected to the D-cap array, forming a single resonant circuit capable of selectively resonating at multiple frequencies controlled via RF control sequences to set and fine tune the chip's capacitance. This work describes the design and measurements of the microchip level D-cap array implemented for a selective wirelessly adjustable multi-frequency probe (4) and Automatic Impedance Matching (AIM) system (see Conference abstract index).

Methods: The D-Cap was designed for the selection and tuning of multiple capacitive values to selectively tune a 20 nH implantable coil to the NMR resonant frequencies of 190 MHz (^{31}P), 442 MHz (^{19}F), and 470 MHz (^{1}H) in an 11.1 Tesla environment. The fabricated chip consists of multiple branches of capacitors of set step sizes connected in series to transistors programmed by an 11-bit digital word, setting the overall capacitance through the digital switching of the transistors, as shown in Fig. 1b. Each branch contains capacitance values ranging from 16 pF to 31.25 fF and the total capacitance seen at the input is equivalent to the sum of the capacitive values of the parallel branches that are turned on and the parasitic capacitance (C_{par}) associated with all the branches that are disabled. The minimum capacitance value that is attainable is therefore related to the parasitic capacitance contributions of the digital switches. To minimize C_{par} and maximize the tuning range, the D-cap utilizes a binary weighted 7-bit fine tuning array and four coarse tuning bits (16 pF, 16 pF, 8 pF and 4-C_{par}) - the smallest fixed capacitance coarse bit was sized to absorb C_{par} and yield a capacitance of ~4 pF.

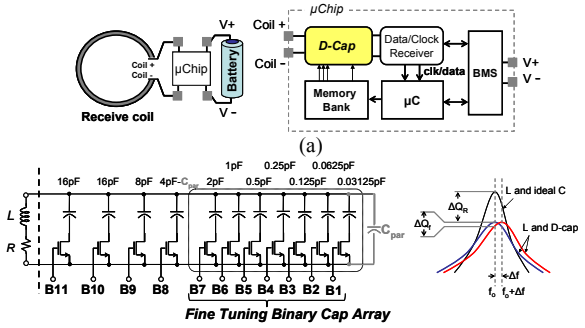

Figure 1. (a) D-cap µChip block diagram (b) D-cap array and (c) Q degradation effects.

The two main loss mechanisms that result from replacing a fixed value capacitor with a digitally controlled capacitor array are illustrated in Fig. 1c. The first and most detrimental loss arises from the finite effective series resistance (ESR) of the digital transistor switches, which degrades the capacitor quality factor (Q) by ΔQ_R. The second loss mechanism, denoted by ΔQ_F, is caused by a finite frequency resolution from discrete capacitance step sizes of the digital capacitor array, and can generally be neglected when the minimum capacitance step size is small relative to the overall desired capacitance. The sizing of a transistor switch is proportional to the parasitic capacitance introduced and inversely proportional to the ESR of the transistor causing a design constraint to make a low ESR to produce good signal sensitivity while reducing the overall parasitic capacitance so as not to limit the highest NMR frequency. In order to address this design constraint the transistors in the lower order capacitance branches were sized for minimal ESR and the higher order capacitance branches with higher ESR. Therefore, the time constants of each branch, defined by the product of the branch ESR and corresponding branch capacitance, were chosen to minimize the degradation in Q at the desired operating frequency.

Results: The prototype D-Cap test chip was fabricated in a 1.2 V, 0.13 µm CMOS process and shown in Fig. 2a. The fully integrated capacitor area measures approximately 600 x 450 µm. Binary capacitance tuning of the D-cap shows a tuning range of 5.5 pF to ~ 60 pF over a wide frequency range (Fig. 2b and 2c). The resolution of the D-cap is ~ 30 fF and the parasitic capacitance is ~ 5.5 pF. Figure 2d shows the quality factor of the D-Cap array vs. frequency at the required capacitances to resonate at 442 MHz and 470 MHz. The unloaded Q was measured to be 27.1 at 442 MHZ and 29.7 at 470 MHz.

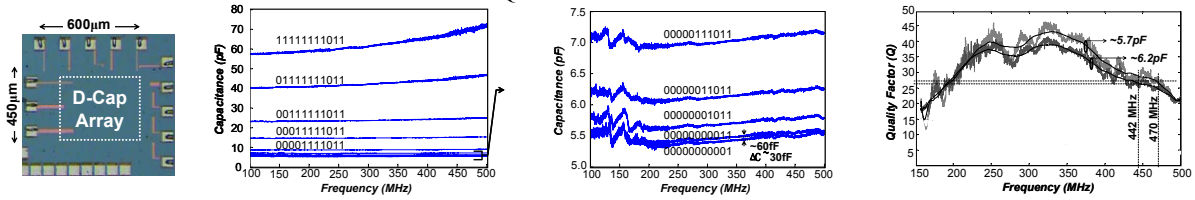

Figure. 2 (a) D-Cap array die photo, (b) measured cap. vs. freq. for larger step sizes (c) and lower step sizes, (d) Q measurements for settings of 5.78 pF and 6.23 pF.

Conclusion: These results validate the overall concept design of the digitally controlled capacitor array chip. The D-Cap is capable of setting a digitally controlled capacitive value to produce a resonant circuit with the NMR coil, which can be set to multiple frequencies. From previous studies, a PDMS-coated coil implanted into mice exhibits a loaded Q of ~15 (3), which if used together with the D-cap would result in a Q degradation of ~33%. This can be improved through the use of a smaller CMOS technology node to produce lower transistor switch ESR, yielding a higher quality factor with reduced parasitic capacitances. Alternatively, the capacitance range can be traded off for a lower switch ESR and higher Q. This test chip design confirms the basic functionality of a digitally controlled capacitor array chip.

References: 1) Lim F, *et al.,* Science 1980; 210(4472):908-910. 2) Sun A, *et al*., Artificial Organs 1980;4(4):275-278. 3) Volland NA, *et al.*, "Development of an inductively-coupled MR coil system for imaging and spectroscopic analysis of an implantable bioartificial construct at 11.1T ", MRM, in press. 4) Beck BL, *et al*., ISMRM 2008, #1116.

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