Optimizing Pin Diode Performance in Transceiver Coils

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Introduction: Pin-diodes are widely used in MRI coils as switching elements. However, in a forward bias condition, they have limited power rating and a resistance which may be comparable to the unloaded coil resistance. The pin-diode resistive loss is not a problem when used as a series element and the loaded coil resistance is dominated by sample losses. However, under some conditions the pin-diode may still decrease coil efficiency. When reverse biased such as when used in a shunt or parallel mode, pin diodes require the RF peak voltage not to exceed the pin diode break down voltage and the reverse bias DC voltage. For many applications, the pin-diode may be operated at a much lower reverse bias DC voltage known as a conditional safe operation. That is when the DC bias voltage is higher than the self-generated DC voltage, which is dependent upon the i-region thickness and RF duty cycle [1]. The self-generated DC voltage is usually determined by experiment. For these reasons, pin-diodes are most often used in a forward bias condition when the RF power is high. For a receive coil, this works well. For a transmit or transceiver coil, it is still desirable to minimize the pin-diode losses. We demonstrate here a parallel pin-diode configuration that overcomes the above problems without requiring high power ratings or high breakdown voltages for the pin-diode.

Theory: As shown in figure 1, the circuit includes a pin-diode D, inductor L2 and L3, and a capacitor C2. L1 is the main coil inductor which resonates with C1 and Ceff at the Larmor frequency f_0. C1 and Ceff are the distributed tuning capacitors and Ceff represents any number of capacitors as long as it satisfies $2\pi f_0 = [(C1^{-1} + Ceff^{-1})^{-1} L1]^{-1/2}$. When the pin-diode D is forward biased, L2 and C2 resonate at f_0 to create a high impedance block, while the main coil resonates at f_0. When D is reverse biased, ideally L3 resonates with C1 and C2 to create a high impedance block that effectively turns off the coil. Under both conditions, the pin-diode, D, will not be exposed to high RF voltage drops.

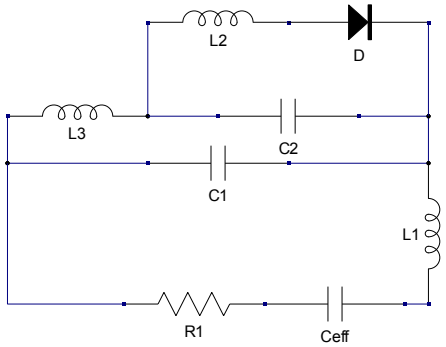

Figure 1 Transceiver coil circuit with new pin-diode configuration

Methods: The isolation of the circuit was simulated and experimentally verified. Experimental measurements were performed on a 3.5 inch diameter reference coil under three conditions; (A) without pin-diode circuit, (B) with a pin-diode in series with C1 and Ceff, and (C) with the pin-diode as shown in Fig. 1. Bench measurements of sensitivity and Q were made with an HP 4195A network analyzer. Sensitivity is defined as the ratio of the received voltage signal from the matched coils (B or C) to the received voltage signal from matched coil (A) utilizing a broadband transmit coil at a fixed distance from the receive coils. SNR measurements were made using a 1ml doped water sample centered in the coil on a Siemens Tim-Trio 3T scanner.

Results and Discussion: At ω_0, the total resistance of the coil in figure 1 is $R1 + (R_D + R_{L2})(C2/C1)^2$ where R_D is the forward bias resistance of D and R_{L2} is L2's resistance. As C2/C1 decreases, the total resistance decreases; however, isolation is optimal at only one value of C2/C1. Thus, the value of C2 is dictated by practical sizes of inductors L2 and L3 and the isolation of the circuit. In the experiment, a 4.7pf was chosen for C2 as it gives the same isolation performance (47.45dB) as the pin-diode in coil B. Table one shows that the measurement results and the differences between Q, sensitivity and SNR measurements are within 10%. Under these conditions SNR and sensitivity are expected to be proportional to $Q^{1/2}$. Since C1 and Ceff may be adjusted, this provides greater flexibility in choosing a C2 value.

Table 1 Measurement Data

	Q value	Normalized ($Q^{1/2}$)	Normalized SNR	Sensitivity	Isolation (dB)
Coil A	370	1	1	1	N/A
Coil B	210	0.75	0.69	0.78	47.4
Coil C	345	**0.97**	1.01	0.95	47.45

Table 2. Component Parameters of Figure 1.

C1	39pf	R1	0.44ohm
C2	4.7pf	R_{L2}	0.86ohm
Ceff	9.86pf	R_{L3}	0.56ohm
L1	0.212uH	R_D	0.34ohm
L2	0.355uH	L3	0.232uH

Conclusion: In this work, a simple pin-diode circuit is designed to maximize the efficiency of the transceiver coil. The results show that this design minimizes the resistive loss due to the pin-diode serial resistance while at the same time provides good isolation. In addition, the pin-diode experiences lower RF voltage drops and power consumption. All of which helps to prevent pin-diode degradation.

Reference: [1] Robert H. Caverly, Gerald Hiller, "Establishing the Minimun Reverse Bias for a p-i-n Diode in a High-Power Switch," IEEE Transactions on Microwave Theory and Techniques, vol. 38, issue 12, pp. 1938-1943