Semiconductive Coated Transverse Gradient Board Increases Partial Discharge Inception Voltage

D. A. Seeber[1], A. Mantone[1], and S. Dong[2]
[1]GE Healthcare, Florence, SC, United States, [2]GE Global Research, Shanghai, China, People's Republic of

Introduction

A partial discharge occurs in a void between two adjacent metal plates. At the partial discharge inception voltage (PDIV) a small spark bridges the void and causes emission of a radio frequency noise burst. An MRI scanner can detect the noise burst and cause artifacts in the MRI image. A MRI gradient coil, consisting of several layers of copper boards and insulation layers, is susceptible to partial discharges if voids are left in the insulation layers during vacuum pressure impregnation (VPI) or due to bonding imperfections. Partial discharges occurring in a gradient coil result in an effect called "white pixels". The bonding imperfections between the epoxy and copper are a source of partial discharge events that can be reduced by coating both sides of the copper surface with a semiconductive laminate layer.

Experimental Test Method

A source of void formation is poor bonding between the copper and the epoxy or the copper surface and fiberglass substrate used in the VPI process. Development of an epoxy that bonds completely to the copper surface is difficult to manufacture, as the epoxy does not bond well to both the inorganic metal and to the organic fiberglass. Also, incomplete coverage during lamination of the copper and fiberglass is susceptible to void trapping as well as bonding difficulties between the copper and the resin in the fiberglass. A method of reducing the effect of voids due to the copper/epoxy interface is to laminate the copper surfaces with a layer of semiconductor, see Figure 1. If delamination occurs between the copper and semiconductor, the void will be surrounded by an equipotential surface and will reduce the electric field stress and the potential to cause a partial discharge event. Additionally, the epoxy in the semiconductor laminate will facilitate bonding with the VPI resin. A carbon-black semiconductive layer with resistance of 10^6-10^9 ohms/square was laminated to both surfaces of a copper sheet used for a transverse gradient coil (~1000 cm by ~600 cm). Two of semiconductor coated boards where then stacked vertically with 0.5 mm of dry glass tape separation with two uncoated copper transverse gradient boards with 1.0 mm of glass tape, inside a mold and impregnated with an epoxy using the VPI process. The vertical distance between the copper layers was measured after the experiment by sectioning the sample and the PDIV voltage was recorded per millimeter of separation. An identical experiment was repeated to check for accuracy. The experiment allows for a semiconductive-semiconductive layer and an uncoated-uncoated layer to be conducted under identical impregnation process for comparison

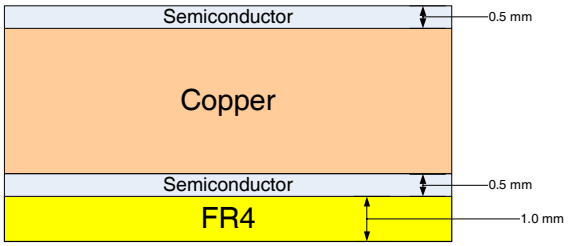

Figure 1. A copper transverse gradient board coated with a semiconductive layer on both surfaces will reduce the effect of voids at interface causing partial discharge.

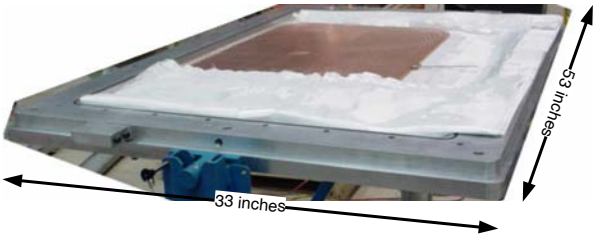

Figure 2. The aluminum mold is shown with the top uncoated transverse gradient board visible along with the dry glass tape separating the bottom board. The mold is then sealed and impregnated with an epoxy and tested for PDIV between the two vertically adjacent copper boards.

Results

The experiments resulted in a 50% increase of the partial discharge inception voltage with the semiconductive layers versus the uncoated copper boards. The results from the two experiments are shown in Figure 3. A scanning electron microscopy was conducted to examine the impregnated sample for voids between the copper and semiconductive layer and between the semiconductive and VPI epoxy/glass layer. Figure 4 demonstrates that no voids exist in the semiconductor sample. The semiconductive laminate on the copper surface increases the PDIV and will consequently reduce the susceptibility to MRI "white pixels" artifacts.

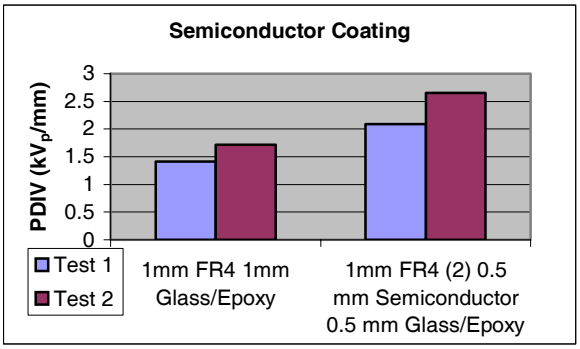

Figure 3. The results of two identical experiments demonstrate the effectiveness of the semiconductive coating to increase the inception voltage by 50%.

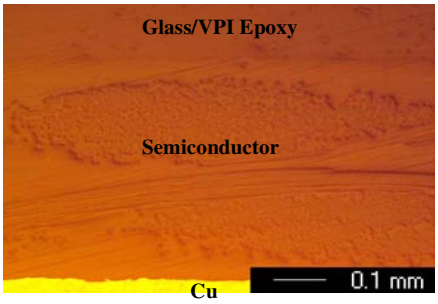

Figure 4. An SEM micrograph does not show any delamination or insulation voids.