A Compact 64 Channel Real-Time MRI Reconstruction System

N. Yallapragada[1], S. M. Wright[1], M. P. McDougall[1]
[1]Dept. of Electrical Engineering, Texas A&M University, College Station, TX, United States

INTRODUCTION: A number of groups have developed systems for real-time reconstruction and display of MR images [1]. Although the feasibility of these systems was demonstrated some time ago [2], the technical challenges are significantly greater for real-time reconstruction and display of images in parallel imaging systems due to the large amounts of data which must be processed. For example, to acquire a 1.28ms echo digitized at a rate of 2.5MHz from a 64 channel receiver would result in 400KB of data generated for every acquisition, which would translate to 48MB of data generated per second for a TR of 8ms. Conventionally, this data had to be stored for all the acquisitions and then processed. This presented to two main disadvantages. Firstly, since the acquisition sizes were huge, the total numbers of acquisitions were limited to a small number by the system memory. Secondly, the image reconstruction had to be done off-line. One group has demonstrated a very robust 32 channel real-time data acquisition system [3]. This system is not widely available, and essentially beyond the capacity of most users to construct. We investigated a compact real-time method to overcome these challenges. This abstract reports a compact real-time data acquisition system capable of real-time demodulation of data from a 64 channel system. The system has been tested with TRs as little as 8ms. Additionally, the system allows periodic update of images on the computer screen, at frame rates of greater than 15 frames per second.

METHOD: Two commercially available digital signal processing (DSP) boards were added to the 64 channel receiver system [4]. The two digitizer boards and the two DSP boards were connected via front panel data port (FPDP) interfaces. The FPDP bus which is capable of data transfers at the rate of 160MB per second was used to move the digitized signal from the digitizer to the DSP board. A block diagram of the hardware setup is shown in Fig. 1. An echo with an intermediate frequency of 500KHz was digitized at 2.5MHz for 1.28ms, i.e. 3200 points per channel were acquired and transferred to the DSP. On the DSP board, digitized signals corresponding to each channel were copied to two buffers. One buffer was multiplied by a sine function and the other by a cosine function. The frequencies of these sinusoidal functions were made equal to the intermediate frequency. The resultant in-phase and out-of-phase signals were convolved with a 50 coefficient FIR filter to extract the lower sideband signal and then the signal was decimated by a factor of 25 (having satisfied the Nyquist criterion). The resultant two signals correspond to the real and imaginary parts of the k-space line represented by the particular channel. This demodulation process (Fig. 2) was repeated for all the 64 channels of an acquisition and over all acquisitions. The challenges involved in this method were two fold. Firstly, the data transfers between the digitizer and the DSP boards have to be in tandem. This was achieved by the means of multi-threaded programming. Second, the demodulation algorithm must be fast enough to facilitate TRs as short as 8ms. This was made possible by doing a ‘selective’ convolution, where in a convolution sum was calculated at only those points which made through the decimation filter. The resultant complex k-space data was either stored in the on-board SDRAM till all acquisitions are processed and then moved to the hard disk for storage. Or, sent out for an on screen display.

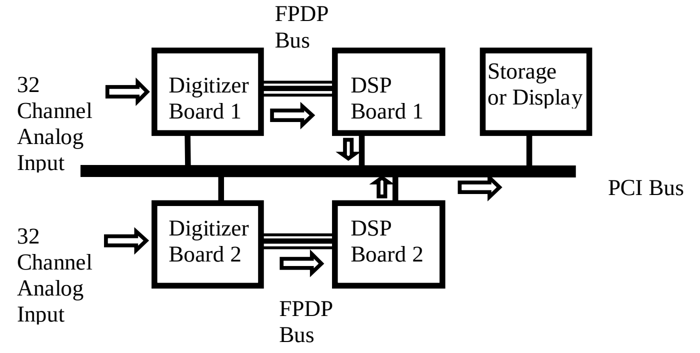

Figure 1: Block diagram of the hardware setup. Two digitizer and two DSP boards were used to acquire and digitally demodulate 64 channel signals in real-time.

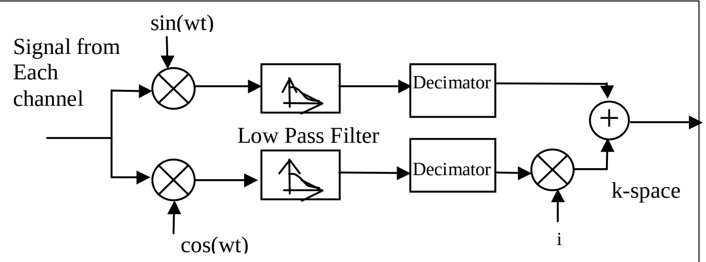

Figure 2: Block diagram of the digital demodulation algorithm executed by the DSP board. Signal from each channel is multiplied by sinusoidal functions (frequency equals the intermediate frequency), low pass filtered and decimated, to obtain complex k-space data.

RESULTS & DISCUSSION: The method was tested with a 64 channel planar array coil for rapid flow imaging [5]. The technique successfully acquired, demodulated and stored the k-space data in the on-board SDRAM for a TR of 8ms (i.e. 125 frames per second). The experiment was carried out for 1 minute before the on-board SDRAM was completely full. The method was also able to display the reconstructed images on the screen at a rate of 15 frames per second. Currently, we are investigating methods to improve this rate. Most importantly, the work has demonstrated that a compact real-time reconstruction system is possible to be built in a single computer.

REFERENCES

[1] Naganawa, S., et.al., Rad. Med,18(1):71-9, 2000
[2] Wright, RC., Magn Reson Med, 12(3):407-15,1989
[3] Hardy, CJ., Magn Reson Med, 52(4):878-84, 2004
[4] Brown, DG., et. al., Proc. ISMRM 10, p. 863,2002
[5] Wright, SM., et. al., Proc. ISMRM 2005 (submitted)

ACKNOWLEDGEMENTS

Support by the Dept. of the Army (DAMD17-97-2-7016) and the National Institutes of Health (1R21EB003296-01A1) is gratefully acknowledged. This paper does not necessarily represent the position or policy of the sponsors.