A 32-Channel Parallel Exciter/Amplifier Transmit System for 7T Imaging

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Introduction:
Parallel transmission (Tx) generalizes conventional Tx and RF shimming, offering extra degrees of freedom and significant opportunities for optimizing Tx performance, improving pulse design trade-off, and leveraging new coil concepts. The present work of developing a 32 Tx-channel system reflects an interest in 1) exploring the opportunities thoroughly and acquiring insights to the question of “what is the optimal number of channels?” and 2) developing state-of-the-art RF sequencer and power amplifier instrumentation. There were significant efforts in recent years prototyping high transmit channel-count research platforms [1,2]. In the following, we describe the RF sequencer and RF power amplifier development efforts and present initial bench testing results.

Methods and Results:
The present approach to a multi-channel, parallel RF sequencer/amplifier (RFSA) design implements a fully contained, stand-alone subsystem which can be preprogrammed with all real-time envelope waveforms and pulse sequences for a given study. This subsystem replaces the existing RF transmit system, so that there are no old/new waveform compatibility issues. The 32-channel system is implemented physically in 8-channel sections. A diagram of the system architecture is shown in Figure 1. Each of the four water-cooled sections in this system includes eight RF power amplifiers and an 8-channel RF sequencer, controlled by an embedded single board computer (SBC). The run time interface requires only three existing real time signals: 1) RF unblank for a safety interlock mechanism; 2) shot trigger for pulse timing; and 3) reference clock for precise frequency synchronization. Software communication is maintained between the host computer and the 32-channel subsystem at all times; with one function being to link all safety interlocks between the existing system and the new RF subsystem. The architecture allows for straightforward configuration of systems with more or fewer channels.

Within each of the 8-channel sections, FPGA’s control the real time clock system, envelope scaling, and interpolation, while the latest generation of high-speed, low-cost RF synthesizer IC’s implement essentially all subsequent RF frequency synthesis: DDS carrier generation, modulation, interpolation, and high speed D/A conversion. With internal clocks up to 1 GHz, these devices generate the 7T, 298 MHZ RF signals directly, without any need for analog mixing and local oscillators.

Discussion/Conclusion:
Initial tests have demonstrated the feasibility of an add-on exciter section without the need to replicate the receiver architecture. This is a research platform that can be integrated with various MR scanner models. It is also a prototype demonstrating the possibility of a new generation of spectrometers that take advantage of modern digital/RF technology from the telecommunication industry. The next steps will be the integration of this RF subsystem with new multi-channel coils for imaging tests.