Multiprocessor System for Real-Time Convolution Interpolation Reconstruction

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Introduction

Real-time magnetic resonance imaging (MRI) has been of increasing interest for a variety of applications that require the visualization of dynamic processes. It necessitates besides a fast acquisition method mostly an immediate reconstruction and display of the measurement. To meet the resulting demand for processing performance, essentially two different approaches have hitherto been pursued. The first relies on commercially available general-purpose workstations or personal computers. Due to their currently insufficient performance, either a distributed system of several such machines or a single multiprocessor system had to be employed [1]. Nevertheless, this approach suffered from a high latency and a low reconstruction rate in case of multiple receive coils or larger image matrices. It provides a flexibly programmable platform, however, and is thus adaptable to different acquisition methods. The second approach is based on dedicated reconstruction hardware. It led to the development of systems with higher performance and lower latency but restricted applicability since they were tailored to either Cartesian [2] or radial imaging [3].

This works aims at combining the advantages of both approaches in one multiprocessor system build of programmable digital signal processors (DSP). It is shown to outperform all previously reported digital reconstruction hardware for MRI while allowing arbitrary acquisition trajectories due to the employed convolution interpolation reconstruction.

Hardware Architecture

Since typical signal processing operations constitute the main computational load of the convolution interpolation reconstruction, DSPs are a particularly well suited hardware platform for its fast execution. However, current single DSPs do not meet the performance requirements of advanced real-time imaging with up to 6 receive coils and 256^2 image matrices. Multiprocessing is thus inevitable. In order to provide the high external memory bandwidth required by the reconstruction, a distributed memory architecture was preferred to a shared one. Analog Devices' SHARC DSP was considered as the most suitable currently available processor for such a system.

Pipelining and parallel processing allow to speed up the convolution interpolation reconstruction. It was therefore divided into four pipeline stages of which the intermediate two, that perform the convolution and the Fourier transform, are each represented by four DSPs processing in parallel.

The system complies with the real-time constraints of the measurement and thus minimizes the latency of the reconstruction. This is especially beneficial to interactive applications. However, the transmission of reconstructed images is decoupled from the measurement and its rate automatically adapts to the connected display. Whenever the display is ready to receive the next image, it will be provided with the last reconstructed one.

The whole system fits on a single printed circuit board of the dimensions 9.1´´ x 8.7´´ and is thus very compact.

Software Architecture

The currently available software comprises a

- Convolution interpolation reconstruction
- Combination of single receive coil images
  - Coarse calibration
  - Sum of squares
- Sliding window reconstruction
- Adaptation of images for display

The implementation of the convolution interpolation reconstruction is based on the gridding algorithm described in [4]. Although the convolution kernel can be specified arbitrarily, only the Kaiser-Bessel window proposed in [5] has been used so far. The required sampling density compensation follows the approach outlined in [6]. Nevertheless, an adaptation to other proposals such as [7] is feasible without substantial modifications.

The order in which the individual parts of the reconstruction are carried out depends on the selected algorithm for combining the single receive coil images. For the coarse calibration [8], the sliding window reconstruction [9] is performed just once for all coils while the sum of squares approach requires, due to its non-linearity, a separate sliding window reconstruction for each coil.

Currently, all parameters the hardware requires are first computed on a host computer during the preparation phase of the measurement and then downloaded to the system. They include

- Index tables representing the trajectory
- Index tables representing the data partition
- Sampling density compensation vectors
- Convolution window and its Fourier transform
- Coil sensitivities

An optimal system performance is assured by balancing the loads of the different pipeline stages and of the DSPs processing in parallel. For this purpose, an adaptive image partition is used which results in a suitable distribution of the acquired samples over the processors. It is optimized using the a priori knowledge of the samples' distribution in the frequency domain.

Results

The performance of the described reconstruction hardware was verified both in a stand-alone set-up as well as integrated into a 1.5 T Gyroscan ACS-NT MR system (Philips Medical Systems, Best, The Netherlands). Different sequences which are of particular interest for real-time imaging such as echo planar, radial and spiral imaging were used for this evaluation. Typically, the acquisition of a complete image was divided into 16 subsets of equal size, and a reconstruction was performed after every partial acquisition.

The system attained in general a reconstruction rate of more than 350 images/s for 128^2 matrices and of more than 100 images/s for 256^2 matrices. It thus exceeds the figures reported for general-purpose systems [1] by more than a factor of 17 and those for special-purpose systems [2] by a factor of 3. Since the reconstruction performance scales almost linearly with the number of used receive coils, the frame rate still remains higher than 25 images/s even when four receive coils and a 256^2 matrix are used.

The overall latency of the reconstruction is in the order of the inverted reconstruction rate, thus typically significantly lower than the 100 ms.

Conclusions

A multiprocessor system build of high performance DSPs has been proposed as a suitable platform for convolution interpolation reconstruction. It offers in comparison to previous dedicated reconstruction hardware higher flexibility, higher performance and more compactness and in comparison to general-purpose reconstruction hardware an order of magnitude higher performance and a significantly lower latency.

References

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